

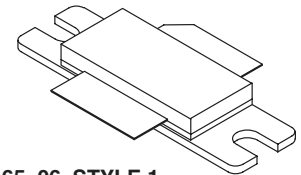
The RF Sub-Micron MOSFET Line  
**RF Power Field Effect Transistors**  
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 921 to 960 MHz, the high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

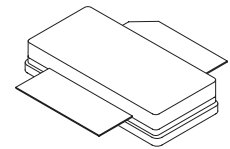
- Typical Performance for GSM Frequencies, 921 to 960 MHz, 28 Volts  
Output Power @ P1dB — 135 Watts  
Power Gain — 16.5 dB @ 130 Watts Output Power  
Efficiency — 48% @ 130 Watts Output Power
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, All Frequency Band, 130 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

**MRF9130L**  
**MRF9130LR3**  
**MRF9130LSR3**

**GSM/EDGE**  
**921-960 MHz, 130 W, 28 V**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465-06, STYLE 1**  
**(NI-780)**  
**(MRF9130L)**



**CASE 465A-06, STYLE 1**  
**(NI-780S)**  
**(MRF9130LSR3)**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	298 1.7	Watts W/°C
Storage Temperature Range	$T_{stg}$	-65 to +200	°C
Operating Junction Temperature	$T_J$	200	°C

**ESD PROTECTION CHARACTERISTICS**

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C7

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

**NOTE – CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**ON CHARACTERISTICS**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 450\ \mu\text{Adc}$ )	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1000\text{ mAdc}$ )	$V_{GS(Q)}$	—	3.6	—	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3\text{ Adc}$ )	$V_{DS(on)}$	—	0.2	0.4	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 9\text{ Adc}$ )	$g_{fs}$	—	12	—	S

**DYNAMIC CHARACTERISTICS (1)**

Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	110	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	4.4	—	pF

**FUNCTIONAL TESTS** (In Motorola Test Fixture)

Power Output, 1 dB Compression Point ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ} = 1000\text{ mA}$ , $f = 921$ and $960\text{ MHz}$ )	$P_{1dB}$	120	135	—	W
Common–Source Amplifier Power Gain ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 130\text{ W}$ , $I_{DQ} = 1000\text{ mA}$ , $f = 921$ and $960\text{ MHz}$ )	$G_{ps}$	15.5	16.5	—	dB
Drain Efficiency ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 130\text{ W}$ , $I_{DQ} = 1000\text{ mA}$ , $f = 921$ and $960\text{ MHz}$ )	$\eta$	43	48	—	%
Input Return Loss ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 130\text{ W}$ , $I_{DQ} = 1000\text{ mA}$ , $f = 921$ and $960\text{ MHz}$ )	IRL	—	–12	–9	dB
Output Mismatch Stress ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 130\text{ W CW}$ , $I_{DQ} = 1000\text{ mA}$ , $f = 921\text{ MHz}$ , $V_{SWR} = 5:1$ , All Phase Angles at Frequency of Tests)	$\Psi$	No Degradation In Output Power Before and After Test			

(1) Part is internally input matched.

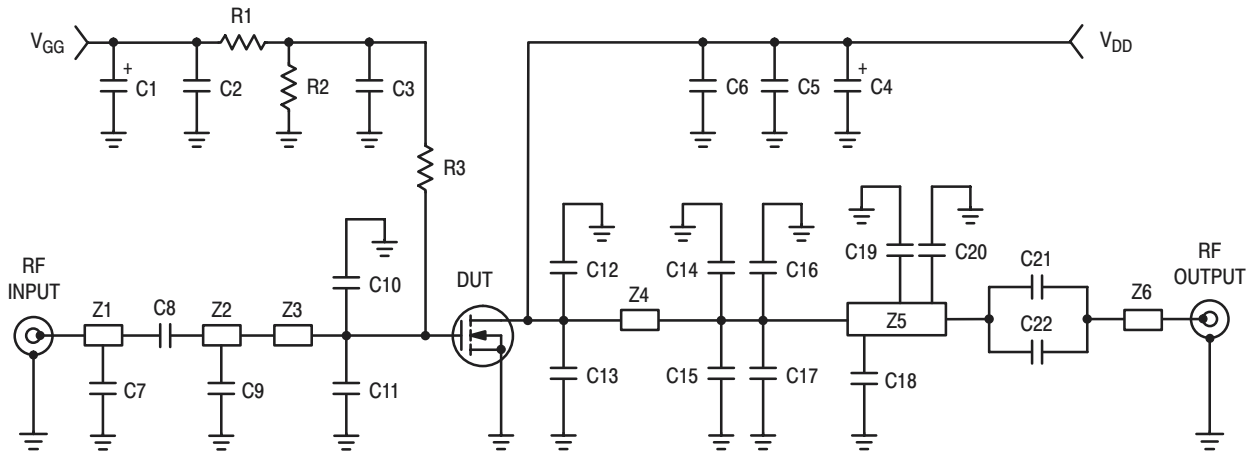


Figure 1. 921–960 MHz Test Circuit Schematic

Table 1. 921–960 MHz Test Circuit Component Designations and Values

Designators	Description
C1, C4	10 $\mu$ F, 35 V Tantalum Capacitors, Vishay–Sprague #293D106X9035D
C2, C5	100 nF Chip Capacitors (1206), AVX #1206C104KATDA
C3, C8, C21, C22	22 pF, 100B Chip Capacitors, ATC #100B220C
C6	33 pF, 100B Chip Capacitor, ATC #100B330JW
C7	1.0 pF, 100B Chip Capacitor, ATC #100B1R0BW
C9	4.7 pF, 100B Chip Capacitor, ATC #100B4R7BW
C10	8.2 pF, 100B Chip Capacitor, ATC #100B8R2CW
C11	10 pF, 100B Chip Capacitor, ATC #100B100GW
C12, C13	12 pF, 100B Chip Capacitors, ATC #100B120GW
C14, C15	2.7 pF, 100B Chip Capacitors, ATC #100B2R7BW
C16, C17, C18	3.9 pF, 100B Chip Capacitors, ATC #100B3R9BW
C19	3.3 pF, 100B Chip Capacitor, ATC #100B3R3BW
C20	1.8 pF, 100B Chip Capacitor, ATC #100B1R8BW
R1	18 k $\Omega$ , 1/8 W Chip Resistor (1206)
R2	10 k $\Omega$ , 1/8 W Chip Resistor (1206)
R3	1.0 k $\Omega$ , 1/8 W Chip Resistor (1206)
Z1	0.117" x 0.600" Microstrip
Z2	0.117" x 1.851" Microstrip
Z3	1.074" x 1.068" Microstrip
Z4	1.074" x 0.980" Microstrip
Z5	0.117" x 1.933" Microstrip
Z6	0.117" x 0.605" Microstrip
Substrate	Taconic TLX8, Thickness 0.8 mm
	RF Connectors, Type N, Macom #3052–1648–10

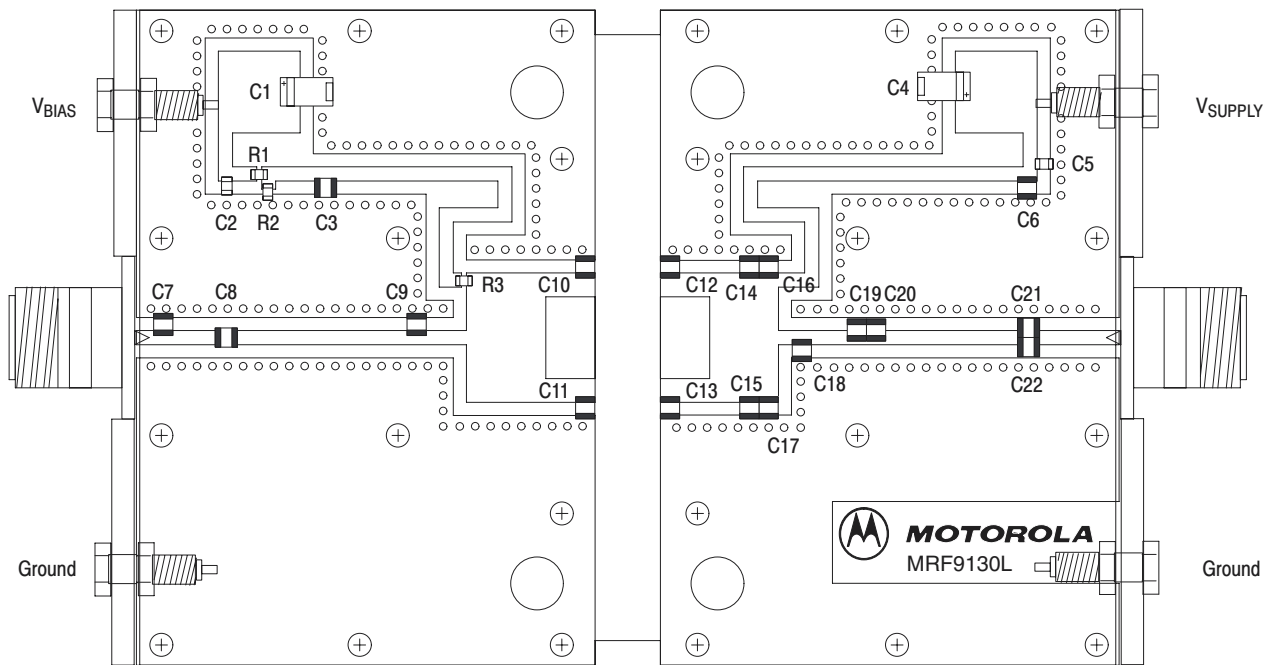
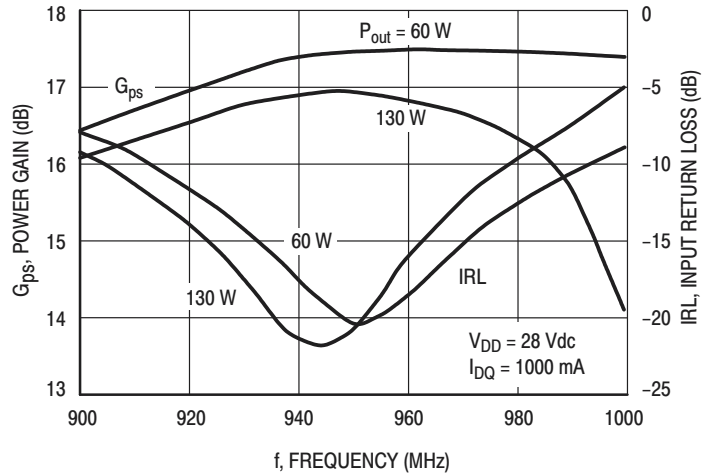
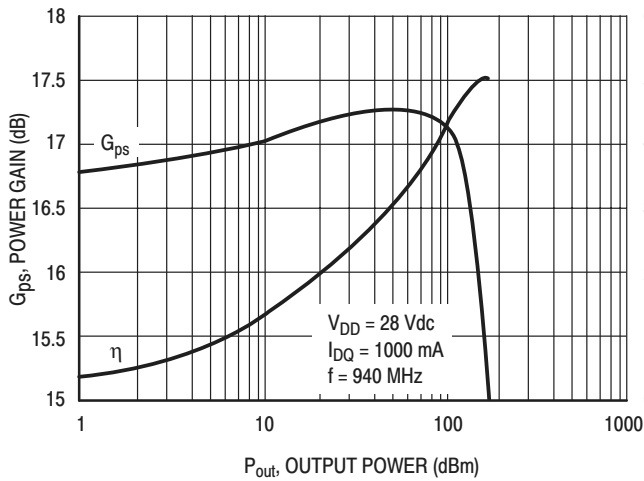


Figure 2. 921–960 MHz Test Circuit Component Layout

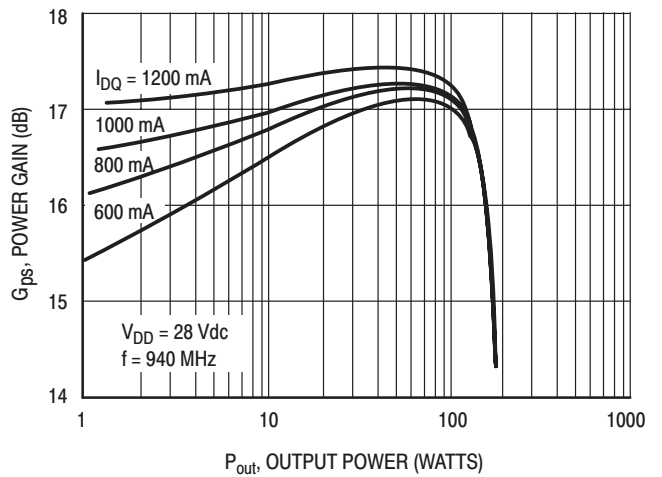
## TYPICAL CHARACTERISTICS



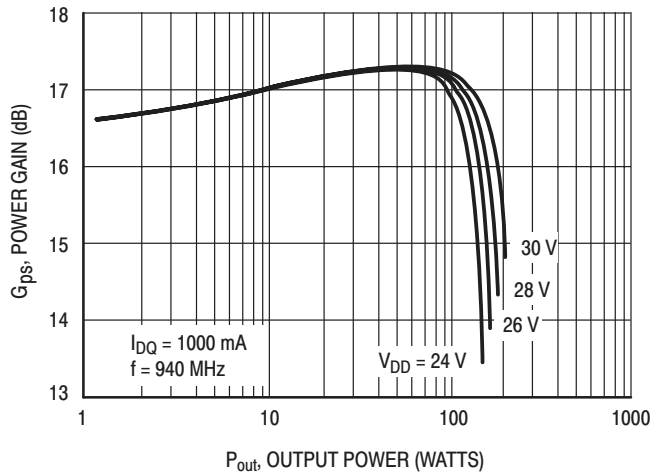
**Figure 3. Power Gain and Input Return Loss versus Frequency**



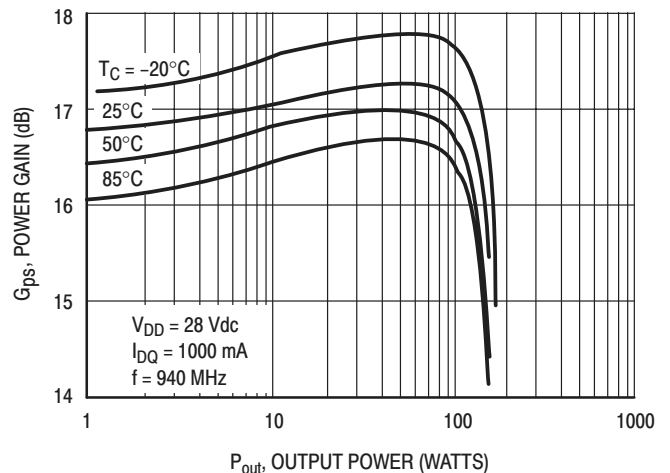
**Figure 4. Power Gain and Efficiency versus Output Power**



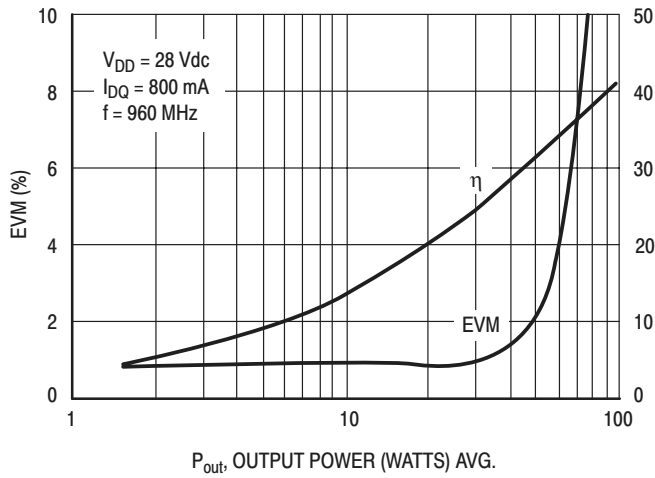
**Figure 5. Power Gain versus Output Power**



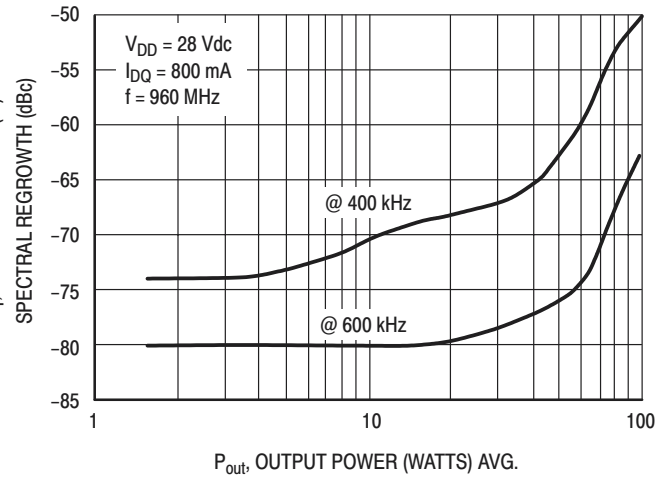
**Figure 6. Power Gain versus Output Power**



**Figure 7. Power Gain versus Output Power**

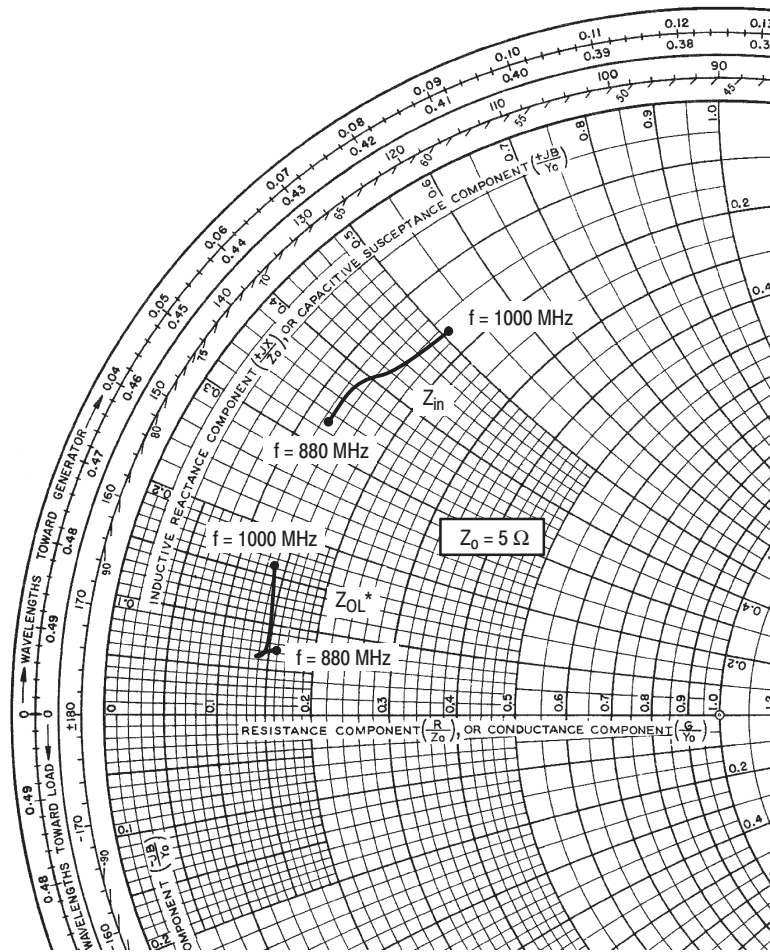


**Figure 8. EVM and Efficiency versus Output Power**



**Figure 9. Spectral Regrowth versus Output Power**

NOTE: Curves on Figure 8 and 9 gathered on a GSM EDGE optimized text fixture.



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1000 \text{ mA}$ ,  $P_{out} = 135 \text{ W (CW)}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
880	$0.63 + j1.66$	$0.82 + j0.36$
920	$0.67 + j1.88$	$0.72 + j0.30$
960	$0.82 + j2.18$	$0.74 + j0.37$
1000	$0.86 + j2.56$	$0.69 + j0.79$

$Z_{in}$  = Complex conjugate of source impedance.

$Z_{OL}^*$  = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note:  $Z_{OL}^*$  was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

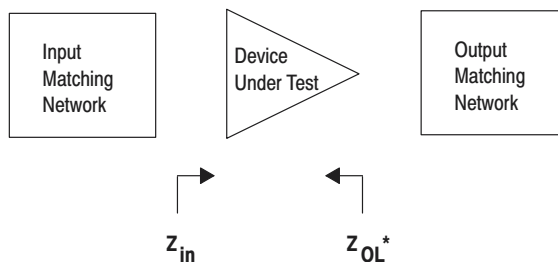


Figure 10. Series Equivalent Input and Output Impedance

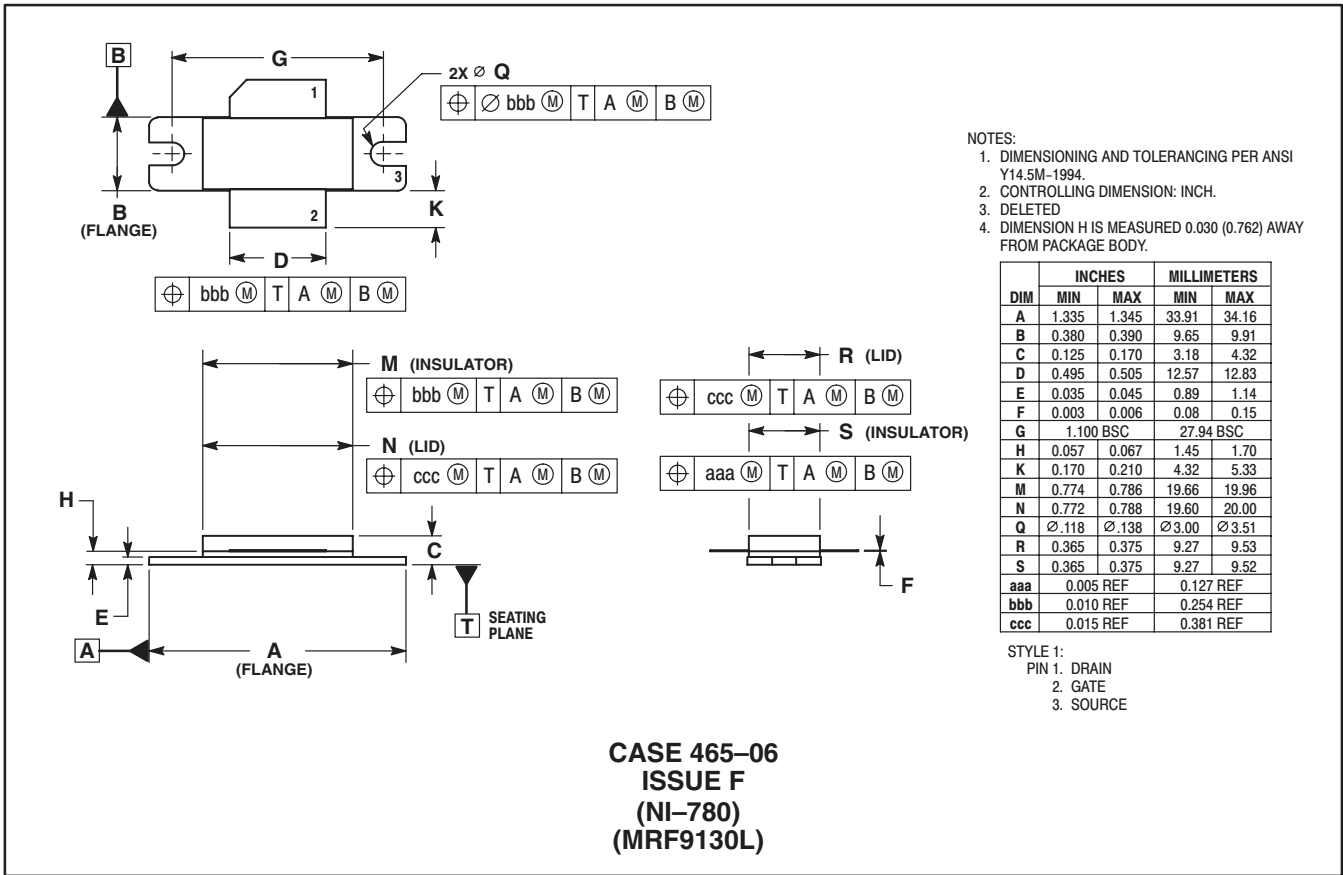
# NOTES



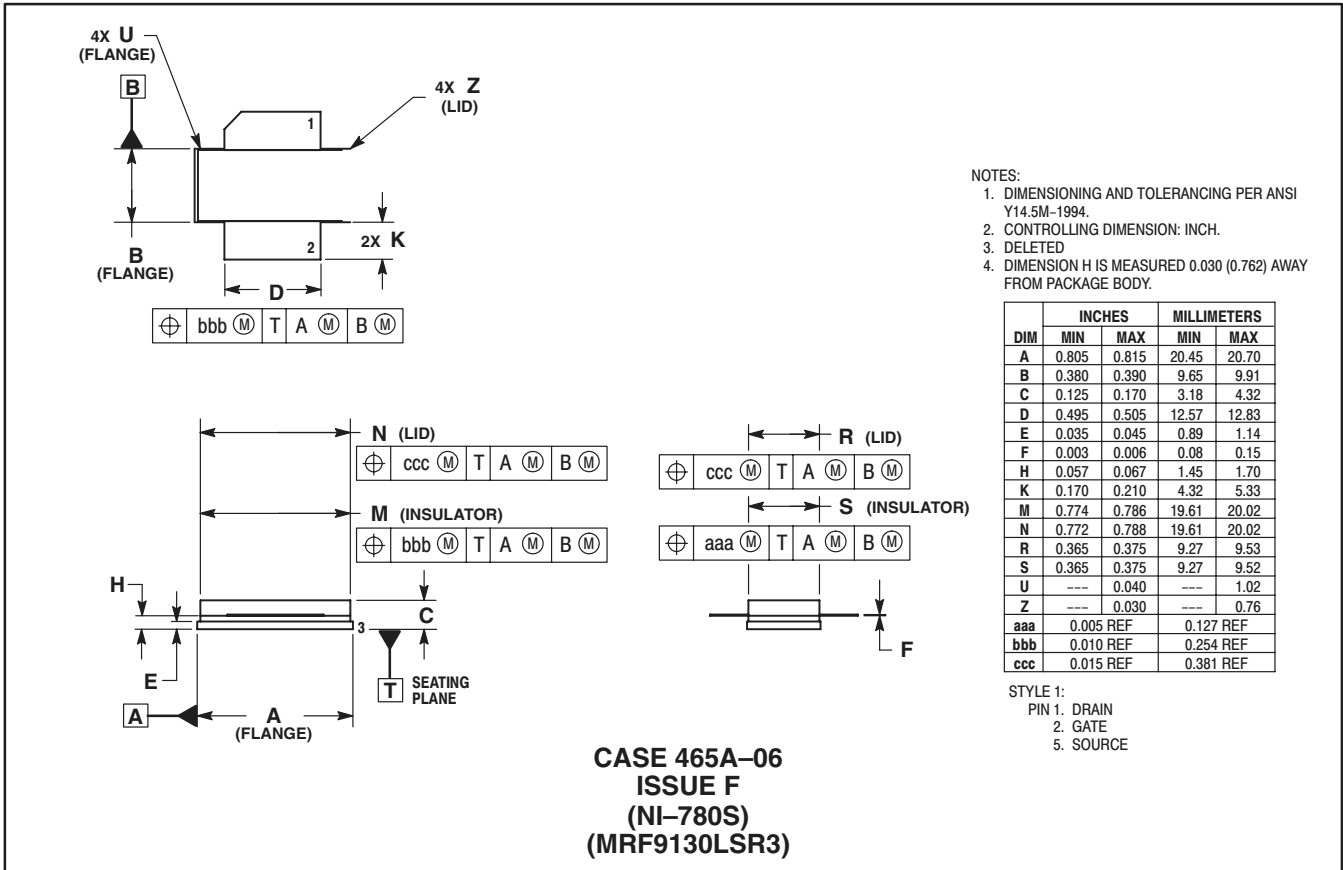
# NOTES

# NOTES


## PACKAGE DIMENSIONS



**CASE 465-06  
ISSUE F  
(NI-780)  
(MRF9130L)**



**CASE 465A-06  
ISSUE F  
(NI-780S)  
(MRF9130LSR3)**

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